KIBABII UNIVERSITY COLLEGE
(A Constituent College of MasindeMuliro University of Science Technology)
P.O. Box 1699-50200 Bungoma, Kenya
Tel. 020-2028660/0708-085934/0734-831729
E-mail: enquiries@kibabiiuniversity.ac.ke

UNIVERSITY EXAMINATIONS
2013/2014 ACADEMIC YEAR

3RD YEAR 2ND SEMESTER EXAMINATIONS

FOR THE DEGREE OF BACHELOR OF COMPUTER SCIENCE

COURSE CODE: CSC 355E

COURSE TITLE: PARALLEL COMPUTER ARCHITECTURE & PROGRAMMING

DATE:16TH APRIL, 2014 TIME: 2:00P.M. – 5:00P.M.

INSTRUCTIONS TO CANDIDATES

- Answer question ONE and any other two questions
- Time Allowed: 3 hours

Section A: Answer ALL questions in this section

Question One (30 marks)

a) Define parallel computer architecture [2 marks]

b) State the three fundamental performance metrics for many design levels [3 marks]

c) The properties of the specified order among operations have a profound effect throughout the layers of parallel architecture. Where the implicit ordering is not enough, explicit synchronization operations are required. Briefly describe two types of synchronization required in parallel programs. [4 marks]

d) Briefly explain each of the following with regard to decomposition and assignment

i) Spatial locality [2 marks]

ii) Temporal locality [2 marks]

iii) Synchronization and granularity [2 marks]

e) Design features in the field of computer architecture are adopted only after detailed evaluations of tradeoffs. Explain four reasons why the job of workload-driven evaluation for multiprocessor architecture is even more difficult than for uniprocessors. [8 marks]

f) Why is the linear scaling property important for a work metric? Illustrate with an example. [4 marks]

g) State the role of **User**, System Software and Hardware in synchronization with regard to the implementation of the internals of high-level synchronization operations such as locks and barriers? [3 marks]

Section B: Answer any TWO questions in this section

Question Two (20 marks)

a) Communication in the Extended Memory Hierarchy is an artifact of how the program is actually implemented and how it interacts with the machine's extended memory hierarchy Explain five sources of this art factual communication. [10 marks]

b) While processors are physical resources, processes provide a convenient way of abstracting or virtualizing a multiprocessor: We initially write parallel programs in terms of processes not physical processors; mapping processes to processors is a subsequent step. With the aid of a well labelled diagram of the step in parallelization, and the relationships among tasks, processes and processors, describe the job of creating a parallel program from a sequential one together with the major performance goals for every step. [10 marks]

Question Three (20 marks)

a) Considering the directory-based systems and cache-coherent systems and the associated hardware-software tradeoffs, explain three limitations of these systems in terms of performance and cost. [6 marks]

b) There are three parts to a complete solution for a relaxed memory consistency model namely the system specification, the programmer's interface, and a translation mechanism. Using relevant examples describe each of the parts. [6 marks]

c) A network is characterized by its topology, routing algorithm, switching strategy, and flow control mechanism. Explain these characteristics with respect to the design of high-performance interconnection networks for parallel computers. [8 marks]

Question Four (20 marks)

a) Distinguish between Sequentially Consistent Execution and Sequentially Consistent system. [2 marks]

b) Briefly explain the major protocol design tradeoffs for consideration during the design of a multiprocessor. [5 marks]

c) The choice of waiting algorithm is quite independent of the type of synchronization. Describe three major components of a given type of synchronization event.

[6 marks]

d) What should a processor that has reached the acquire point do while it waits for the release to happen?? (7 marks]