



**KIBABII UNIVERSITY COLLEGE**

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**UNIVERSITY REGULAR EXAMINATIONS**

**2013/2014 ACADEMIC YEAR**

**1<sup>ST</sup> YEAR 1<sup>ST</sup> SEMESTER EXAMINATIONS**

**FOR THE DEGREE  
OF  
POST GRADUATE DIPLOMA IN IT**

**COURSE CODE: PGD 713**

**COURSE TITLE: INTRODUCTION TO DIGITAL LOGIC**

**DATE: 24<sup>TH</sup> APRIL, 2014**

**TIME: 9:00A.M.-12 NOON**

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**INSTRUCTIONS**

- Answer **QUESTION ONE** and attempt **ANY OTHER TWO** questions from the following five questions

- 1(a) Distinguish between the following
- I combinational and sequential circuits
  - ii register and memory
  - iii a digital and analogue signal
- 6 marks
- (b) A binary pattern is given as 1001011101010100 determine its decimal equivalent if the pattern is considered to be a:
- I BCD number
  - ii Excess three BCD
  - iii signed binary
- 3 marks
- (c) Convert the following decimal numbers to binary
- I 567
  - ii 47.25
- 4 marks
- d) State any TWO features that can be used to evaluate the performance of logic families
- 2 marks
- e) With aid of truth table determine the output expression implement even parity bit for a four input binary bit.
- 5 marks
- 2(a) With the aid of a truth table show that sums part of a full adder circuit can be implemented using exclusive all only and hence implement the full adder
- 14 marks
- (b) Distinguish between
- I min term and maximum term
  - ii parallel adder and serial adder
  - iii Positive and Negative logic
- 6 marks
- 3(a) With aid of a circuit diagram and truth table explain the operation of 3 input TTL NAND gate.
- 10 marks
- (b) Explain any two problems associated with the totem pole output
- 4 marks
- (c) A TTL NAND gates has the following output parameters  
 $I_{OH} = 500\mu A$ ,  $I_{IH} = 50\mu A$  and  $I_{OL} = 16mA$ ,  $I_{IL} = 0.8 mA$  determine the fan out for :
- I High output
  - ii low output
- 6 marks
- 4(a) With aid of circuit diagram and truth table explain the principle operation of RS NAND gate flip flop
- 10 marks
- (b) With aid a timing waveform and logic circuit implement a modulo 10 synchronous counter
- 10 marks
- 5(a) Distinguish between the following
- I a ring counter and Johnson counter
  - ii PIPO register and SIPO
- 4 marks

- (b) Data is received over common line but has to be distributed over four devices.  
With aid of truth table Implement logic circuit to solve this problem 10 marks
- (c) Map on K-Map the exclusive OR function as Sum Of Products and as Product of Sums 6 marks